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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,539	JACKSON ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8-11,15-21 and 23-28* is/are rejected.

7)☒ Claim(s) *2-4,7,12-14 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/18/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on June 18, 2001 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings are objected to because the reference numbers and reference labels are not clear enough to be legible in every case. Further, in figure 3, the reference 32 to the sigma-delta modulator cited in paragraph 28 (pg. 8) of the specification is not shown. Rather, in figure 3, reference 82 is noted as the sigma-delta modulator, and no reference number 32 is found. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top

margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim claims 3, 7, 14, and 16 are objected to because of the following informalities:

Regarding claim 3, the claim provides for a second finite impulse response (FIR) filter. However, claim 2, which is a parent claim of claim 3, provides for a delay circuit. According to the specification and drawings, the FIR filter provides the delay as claimed in claim 2. Therefore, claim 3 is objected to because the second finite impulse response filter conflicts with the delay circuit of claim 2.

Regarding claim 7, in line 3, "generating an output signal" should be replaced by –generating the second output signal—for consistency of the claim language and the embodiment of the invention according to the specification and drawings.

Regarding claim 14, in line 3, "generating an output signal" should be replaced by –generating the second output signal—for consistency of the claim language and the embodiment of the invention according to the specification and drawings.

Regarding claim 16, the claim should be dependent upon claim 11 rather than claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 6, 8-11, 15-21, and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Loughlin (US 5705959) in view of Riley (US 4965531), and in further view of Dent (US 5351016).

Regarding claim 1, O'Loughlin discloses by figure 7 a modulator comprising: a complex modulator (abstract; fig. 7, refs. 71-75), said modulator operative for receiving input data (f(t)) and generating a first output signal (output of 75) representing the modulation to be imposed on a carrier signal to effect complex modulation of said input signal ($\Phi(t)$) and a second output signal (output of 74) representing an amplitude of said input data (a(t)); a frequency or phase modulator (63) and an amplifier (67) for amplifying said carrier signal output by said phase-lock loop circuit, said second output signal controlling the amount of gain of said amplifier (col. 7, line 63 – col. 8, line 43). O'Loughlin discloses a frequency or phase modulator but does not explicitly disclose that the frequency modulator comprises: a sigma-delta modulator and a phase-lock loop circuit. However Riley teaches by figure 1 a sigma-delta modulator (102), said frequency modulator operative for receiving said first output signal (122) generated by said complex modulator, and generating a control signal (104) representing the desired frequency of said carrier signal such that said carrier signal represents said input signal complex modulated; a phase-lock loop circuit (refs. 110, 114, 118, and 106) comprising

a voltage controlled oscillator (118) for generating said carrier signal and a programmable frequency divider (106), said programmable frequency divider receiving said control signal (104) as an input signal, said programmable frequency divider operative for changing the frequency of the carrier signal in accordance with said control signal. The first output signal of O'Loughlin (output of 75) would be applied to the input (122) of the sigma-delta modulator of Riley. Riley further teaches an advantage of the disclosed sigma-delta modulator being that spurious noise generated by a conventional modulator is offset above the wanted frequencies (col. 3, lines 29-34; col. 4, lines 44-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a sigma-delta type frequency/phase modulator as taught by Riley in place of the phase modulator of O'Loughlin because it would offset spurious noises during modulation.

Further regarding claim 1, O'Loughlin in view of Riley disclose complex modulation (offset QPSK modulation is a type of complex modulation) but not explicitly offset QPSK modulation. However, Dent teaches offset QPSK modulation, and teaches that offset QPSK modulation has less envelope fluctuations (col. 2, lines 49-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to use offset QPSK modulation as taught by Dent in the complex modulator of O'Loughlin in view of Riley because the lower envelope fluctuations may advantageously lead to a more linear output. Additionally, at the time the invention was made, it would have been obvious to a person having ordinary skill in the art to utilize offset QPSK as the type of complex modulation utilized by O'Loughlin in

view of Riley. The applicant has not disclosed that the use of offset QPSK provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well using offset QPSK modulation because it is a type of complex modulation having low envelope fluctuations.Regarding claim 6, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 1 as applied above. Further, Riley discloses that said control signal is programmable so as to allow said voltage controlled oscillator to be controlled to a desired carrier frequency. According to figure 1 of Riley, the control signal (104) output from the sigma-delta modulator (102) controls the ratio of the divider (106). In turn, the phase detector will control the VCO (118) through the low pass filter (114) according to the change in the divider output (108) in relation to the reference input (f_i). Therefore, the control signal of the sigma-delta modulator controls the desired carrier frequency output by the VCO in a manner well known and understood by one having ordinary skill in the art.

Regarding claim 8, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 1 as applied above. Further, as understood by one having ordinary skill in the art, the carrier signal output by said phase-lock loop circuit has a constant envelope amplitude. The output of the VCO (Riley; fig. 1, ref. 120) will not vary in amplitude according to the operation of a VCO. Rather, the output will vary only in frequency/phase according to the input (fig. 1, ref. 116). Because the output of the VCO does not change in amplitude, it has a constant envelope amplitude output.

Regarding claim 9, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 1 as applied above. Further, the amplifier (O'Loughlin; fig. 7, ref. 67) operates to amplitude modulate said carrier signal output by said phase-lock loop (Riley; fig. 1, ref. 120) in accordance with the value of said second output signal (O'Loughlin, fig. 7, output of 74).

Regarding claim 10, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 9 as applied above. Further, the amplifier outputs a linearized offset QPSK modulated signal (col. 1, lines 42-60). The purpose of the modulator of O'Loughlin, as understood by one having ordinary skill in the art, is to effect a linear modulation by separately applying phase and amplitude information to a carrier as illustrated by O'Loughlin in figure 7.

Regarding claim 11, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 11 as applied to claim 1 above.

Regarding claim 15, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 11 as applied above. Further, O'Loughlin in view of Riley, and in further view of Dent disclose the additional limitations of claim 15 as applied to claim 8 above.

Regarding claim 16, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 11 as applied above. Further, O'Loughlin in view of Riley, and in further view of Dent disclose the additional limitations of claim 16 as applied to claim 9 above.

Regarding claim 17, O'Loughlin discloses a complex modulator (abstract) comprising: means for receiving an input data signal (f(t)) to be modulated (71); means (75) for generating a digital output signal (output of 75) representing the modulation to be imposed on a carrier signal to effect complex modulation of said input data signal; means (74) for generating an amplitude signal (output of 74) indicative of the amplitude of said input data signal; frequency or phase modulator means (63) for receiving said digital output signal and generating a digital control signal (output of 63) representing the desired frequency of said carrier signal such that said carrier signal represents said input data signal complex modulated; and means (67) for amplifying said carrier signal in accordance with the level of said amplitude signal (col. 7, line 63 – col. 8, line 43). O'Loughlin discloses means for frequency or phase modulating but does not explicitly disclose that the frequency modulator means comprises: means for controlling a programmable frequency divider forming a portion of a phase-lock loop circuit, said programmable frequency divider receiving said digital control signal as an input signal, said programmable frequency divider operative for changing the frequency of said carrier signal in accordance with said control signal, said carrier signal being generated by a voltage controlled oscillator. However, Riley does disclose by figure 1, means for controlling (102) a programmable frequency divider (106) forming a portion of a phase-lock loop circuit (refs. 110, 114, 118, and 106), said programmable frequency divider receiving said digital control signal (104) as an input signal, said programmable frequency divider operative for changing the frequency of said carrier signal in accordance with said control signal, said carrier signal being generated by a voltage

controlled oscillator (118). The first output signal of O'Loughlin (output of 75) would be applied to the input (122) of the sigma-delta modulator of Riley. Riley further teaches an advantage of the disclosed sigma-delta modulator being that spurious noise generated by a conventional modulator is offset above the wanted frequencies (col. 3, lines 29-34; col. 4, lines 44-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a sigma-delta type frequency/phase modulator means as taught by Riley in place of the phase modulator means of O'Loughlin because it would offset spurious noises during modulation.

Further regarding claim 17, O'Loughlin in view of Riley disclose complex modulation (offset QPSK modulation is a type of complex modulation) but not explicitly offset QPSK modulation. However, Dent teaches offset QPSK modulation, and teaches that offset QPSK modulation has less envelope fluctuations (col. 2, lines 49-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to use offset QPSK modulation as taught by Dent in the complex modulator means of O'Loughlin in view of Riley because the lower envelope fluctuations may advantageously lead to a more linear output. Additionally, at the time the invention was made, it would have been obvious to a person having ordinary skill in the art to utilize offset QPSK as the type of complex modulation utilized by O'Loughlin in view of Riley. The applicant has not disclosed that the use of offset QPSK provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform

equally well using offset QPSK modulation because it is a type of complex modulation having low envelope fluctuations.Regarding claim 18, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 17 as applied above. Further, as understood by one having ordinary skill in the art, the carrier signal output by said phase-lock loop circuit means has a constant envelope amplitude. The output of the VCO (Riley; fig. 1, ref. 120) will not vary in amplitude according to the operation of a VCO. Rather, the output will vary only in frequency/phase according to the input (fig. 1, ref. 116). Because the output of the VCO does not change in amplitude, it has a constant envelope amplitude output.

Regarding claim 19, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 17 as applied above. Further, the digital output signal illustrated by O'Loughlin (fig. 7, output of ref. 75) does not contain amplitude information of the data signal. Rather, it contains only phase information, and the output of the amplitude means (74) contains the amplitude information.

Regarding claim 20, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 17 as applied above. Further, the amplifier outputs a linearized offset QPSK modulated signal (col. 1, lines 42-60). The purpose of the modulator of O'Loughlin, as understood by one having ordinary skill in the art, is to effect a linear modulation by separately applying phase and amplitude information to a carrier as illustrated by O'Loughlin in figure 7.

Regarding claim 21, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of the claim as applied to claim 1 above.

Regarding claim 23, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 21 as applied above. Further, Riley discloses the additional limitations of claim 23 as applied to claim 6 above.

Regarding claim 24, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 21 as applied above. Further, Riley discloses the additional limitations of claim 24 as applied to claim 8 above.

Regarding claim 25, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 21 as applied above. Further, Riley discloses the additional limitations of claim 25 as applied to claim 9 above.

Regarding claim 26, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of claim 25 as applied above. Further, Riley discloses the additional limitations of claim 26 as applied to claim 10 above.

Regarding claim 27, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of the claim as applied to claim 17 above.

Regarding claim 28, O'Loughlin in view of Riley, and in further view of Dent disclose the limitations of the claim as applied to claim 1 above.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Loughlin in view of Riley, in further view of Dent, and in further view of Clark (US 5787135).

Regarding claim 5, O'Loughlin in view of Riley, and in further of Dent disclose the limitations of claim 1 as applied above. Further, Riley discloses by figure 1 that said phase-lock loop circuit further comprises: a phase detector (110) coupled to said

programmable frequency divider (106), said phase detector operative for generating an error signal (108) indicating the frequency difference between a reference signal and a signal output by said programmable frequency divider; and a filter (114) coupled to the output of said phase detector. O'Loughlin in view of Riley, and in further view of Dent do not explicitly disclose a reference divider operative for reducing the frequency of a reference signal by a predetermined factor generating an input to the phase detector. However, Clark teaches a reference divider (fig. 1, ref. 12) of a reference generator (fig. 1, "REF IN") having an output applied to a phase detector (fig. 1, ref. 14). The reference divider of Clark is applied, as understood by one having ordinary skill in the art, to create a specific and accurate frequency output by dividing a reference signal. The output of the reference divider may be adjustable and is more stable than the reference signal taken directly. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a reference divider as taught by Clark between the input reference and the phase detector of Riley in the modulator of O'Loughlin in view of Riley and in further view of Dent because the reference divider could be used to supply an adjustable frequency signal which is more stable and accurate than a reference signal taken directly from a reference generator.

Allowable Subject Matter

7. Claims 2-4, 7, 12-14, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references not cited above are cited to further show the state of the art with respect to linearized complex modulators.

U.S. Pat. No. 6489846 to Hatsugai.

U.S. Pat. No. 4972440 to Ernst et al.

U.S. Pat. No. 6590940 to Camp et al.

U.S. Pat. No. 6377784 to McCune.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
February 7, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER